

Appl. No. 10/604,362
Amdt. dated August 29, 2005
Reply to Office action of July 12, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 (currently amended): A power supply clamp circuit for preventing damage to integrated
5 circuits when electrostatic discharge occurs at a first voltage source of the integrated
circuits, the power supply clamp circuit comprising:
a first voltage generator electrically connected to a first node for generating a
voltage;
a first PMOS transistor having a source electrically connected to the first voltage
10 source, a gate electrically connected to the first node, and a drain electrically
connected to a second node;
a first NMOS transistor having a drain electrically connected to the second node, a
gate electrically connected to the first node, and a source connected to ground;
a second NMOS transistor having a drain electrically connected to the first voltage
15 source, a gate electrically connected to the second node, and a source connected
to ground; and
a second PMOS transistor having a source electrically connected to the second node,
a gate and a drain both electrically connected to the first node.
- 20 2 (original): The power supply clamp circuit of claim 1 wherein a drain of the second
NMOS transistor of the power supply clamp circuit has P+ implantation dosage in
an ion implantation process.
- 25 3 (original): The power supply clamp circuit of claim 1 wherein the first voltage generator
of the power supply clamp circuit comprises:
a resistor having one end of the resistor electrically connected to the first voltage

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source and another end of the resistor electrically connected to the first node;
and

a capacitor having one end of the capacitor electrically connected to the first node
and another end of the capacitor connected to ground.

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4 (original): The power supply clamp circuit of claim 3 wherein the resistor of the first
voltage generator comprises metal wiring.

10 5 (original): The power supply clamp circuit of claim 3 wherein the capacitor of the first
voltage generator comprises an NMOS transistor having a drain and a gate
electrically connected to a substrate.

15 6 (currently amended): The power supply clamp circuit of ~~claim 4~~ claim 12 wherein the
~~integrated circuits of the power supply clamp circuit further comprise a second-~~
~~voltage source that is independent from the first voltage source but with the same-~~
~~voltage as the first voltage source, the second voltage source comprising~~ comprises:
a resistor with one end of the resistor electrically connected to the second voltage
source and another end of the resistor electrically connected to a third node;
a third PMOS transistor having a source electrically connected to the third node, a
20 gate electrically connected to a fourth node, and a drain electrically connected to
the first node; and
a third NMOS transistor having a drain and a gate commonly electrically connected
to the fourth node, and a source connected to ground.

25 7 (original): The power supply clamp circuit of claim 6 wherein a drain of the second
NMOS transistor of the power supply clamp circuit has P+ implantation dosage in
an ion implantation process.

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8 (original): The power supply clamp circuit of claim 6 wherein the resistor of the second voltage source comprises metal wiring.

- 5 9 (currently amended): A power supply clamp circuit for preventing damage to integrated circuits when electrostatic discharge occurs at a first voltage source of the integrated circuits, the power supply clamp circuit comprising:
- a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to a first node, and a drain electrically connected to a second node;
 - 10 a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground;
 - a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground;
 - 15 a second voltage source being independent from a first voltage source and having the same voltage as the first voltage source;
 - a resistor with one end of the resistor electrically connected to the second voltage source and another end of the resistor electrically connected to a third node;
 - a ~~third~~ second PMOS transistor having a source electrically connected to the third node, a gate electrically connected to a fourth node, and a drain electrically connected to the first node; and
 - 20 a third NMOS transistor having a drain and a gate commonly electrically connected to the fourth node, and a source connected to ground.
- 25 10 (currently amended): The power supply clamp circuit of ~~claim 8~~ claim 9 wherein the drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

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11 (currently amended): The power supply clamp circuit of ~~claim 8~~ claim 9 wherein the resistor of the power supply clamp circuit comprises metal wiring.

5 12 (new): The power supply clamp circuit of claim 1 further comprising a second voltage source that is independent from the first voltage source but with the same voltage as the first voltage source.